In the Claims:

Currently
~~Cancel~~ amend claims 22-38-49, 51-54 and 56-60. The claims are as follows:

1. (Original) A method of manufacturing an interconnect, comprising:

(a) providing a substrate;

(b) forming a dielectric layer on said substrate;

(c) forming a wire in said dielectric layer, a top surface of said wire coplanar with a top surface of said dielectric layer;

(d) forming a first capping layer on said top surface of said wire and said top surface of said dielectric layer, said first capping layer thin enough to allow penetration of said first capping layer by a point of a conductive probe tip in order to make electrical contact to said wire; and

(e) after step (d) forming a second capping layer on a top surface of said first capping layer.

2. (Original) The method of claim 1, wherein said wire includes copper exposed to an ambient atmosphere at said top surface of said wire.

3. (Original) The method of claim 2, wherein said first capping layer is sufficiently thick to prevent formation, on said top surface of said wire, of copper containing particles by reaction of said wire with said dielectric layer.

4. (Original) The method of claim 1, wherein said dielectric layer comprises fluorinated silicon glass.

5. (Original) The method of claim 4, wherein said dielectric layer comprises about 1% to about 9% by weight of fluorine.

6. (Original) The method of claim 4, wherein said wire includes copper exposed to an ambient atmosphere at said top surface of said wire.

7. (Original) The method of claim 6, wherein said first capping layer is sufficiently thick to prevent formation , on said top surface of said wire, of copper containing particles by reaction of copper in said wire with fluorine in said dielectric layer.

8. (Original) The method of claim 1, wherein said first capping layer and said second capping layer independently include a material selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

9. (Original) The method of claim 1, wherein said first capping layer and said second capping layer independently include one or more layer of materials selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

10. (Original) The method of claim 1, wherein said first capping layer has a thickness between about 100 Å and 300 Å.

11. (Original) The method of claim 1, wherein said second capping layer has a thickness between about 150 Å and 700 Å.

12. (Original) The method of claim 1, wherein said second capping layer is a copper diffusion barrier.

13. (Original) The method of claim 1, wherein said first capping layer in combination with said second capping layer is a copper diffusion barrier.

14. (Original) The method of claim 1, further including:

(f) forming another dielectric layer on a top surface of said second capping layer, said second capping layer acting as a reactive ion etch stop for etching said another dielectric layer.

15. (Original) The method of claim 1, wherein forming said first capping layer comprises forming silicon nitride by high density plasma deposition and forming said second capping layer comprises forming silicon nitride formed by plasma enhanced chemical vapor deposition.

16. (Original) The method of claim 1, further including between steps (d) and (e), cleaning said top surface of said first capping layer.

17. (Original) The method of claim 1, further including between steps (d) and (e), cryogenically cleaning said top surface of said first capping layer.

18. (Original) The method of claim 1, further including between steps (c) and (d), cleaning said top surface of said wire and said top surface of said dielectric layer in a reducing environment.

19. (Original) The method of claim 1, further including between steps (d) and (e), performing one or more characterization procedures selected from the group consisting of optical or SEM inspection and optical or SEM image size measurement.

20. (Original) The method of claim 1, wherein said first capping layer is thin enough to be transparent to visible light, to back-scattered electrons in a SEM or to both.

21. (Original) The method of claim 1, wherein said second capping layer is formed at a temperature of about 350°C or greater

22. (Currently Amended) A method of manufacturing an ~~integrated circuit~~ a structure, comprising:

(a) providing a substrate;

(b) forming a copper diffusion barrier layer on said substrate;

(c) forming a dielectric layer on a top surface of said copper diffusion barrier layer;

(d) forming a copper damascene or dual damascene wire in said dielectric layer, a top surface of said copper damascene or dual damascene wire coplanar with a top surface of said dielectric layer;

(e) forming a first capping layer on said top surface of said wire and said top surface of said dielectric layer;

(f) after step (c) performing one or more characterization procedures in relation to said ~~integrated circuit~~ structure; and

(g) after step (f) forming a second capping layer on said top surface of said first capping layer.

23. (Currently Amended) The method of claim ~~21~~ 22, wherein said dielectric layer comprises fluorinated silicon glass.

24. (Currently Amended) The method of claim ~~22~~ 23, wherein said dielectric layer comprises about 1% to about 9% by weight of fluorine.

25. (Currently Amended) The method of claim ~~23~~ 24, wherein said first capping layer is sufficiently thick to prevent formation, on said top surface of said wire, of copper containing particles by reaction of copper in said wire with fluorine in said dielectric layer.

26. (Currently Amended) The method of claim ~~21~~ 22, wherein said first capping layer and said second capping layer independently include a material selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

27. (Currently Amended) The method of claim ~~21~~ 22 wherein said first capping layer and said second capping layer independently include one or more layer of materials selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

28. ((Currently Amended) The method of claim ~~21~~ 22, wherein said first capping layer has a thickness between about 100 Å and 300 Å.

29. (Currently Amended) The method of claim ~~21~~ 22, wherein said second capping layer has a thickness between about 150 Å and 700 Å.

30. (Currently Amended) The method of claim ~~21~~ 22, wherein said second capping layer is a copper diffusion barrier.

31. (Currently Amended) The method of claim ~~21~~ 22, wherein said first capping layer in combination with said second capping layer is a copper diffusion barrier.

32. (Currently Amended) The method of claim ~~21~~ 22, further including:

(h) forming another dielectric layer subsequently formed on a top surface of said second capping layer, said second capping layer acting as a reactive ion etch stop for etching said another dielectric layer.

33. (Currently Amended) The method of claim ~~21~~ 22, wherein forming said first capping layer comprises forming silicon nitride by high density plasma deposition and forming said second capping layer comprises forming silicon nitride by plasma enhanced chemical vapor deposition.

34. (Currently Amended) The method of claim ~~21~~ 22, further including between steps (f) and (g), cryogenically cleaning said top surface of said first capping layer.

35. (Currently Amended) The method of claim ~~21~~ 22, further including between steps (d) and (e), cleaning said top surface of said wire and said top surface of said dielectric layer in a reducing environment.

36. (Currently Amended) The method of claim ~~21~~ 22, wherein said one or more characterization procedures are selected from the group consisting of optical or SEM inspection, optical or SEM image size measurement and electrical probing.

37. (Currently Amended) The method of claim ~~21~~ 22, wherein said first capping layer is thin enough to be transparent to visible light, to back-scattered electrons in a SEM or to both.

38. (Currently Amended) The method of claim ~~21~~ 22, wherein said first capping layer is thin enough to allow penetration of said first capping layer by a point of a conductive probe tip in order to make electrical contact to said wire.

39. (Currently Amended) ~~An integrated circuit~~ A structure, comprising:

a copper damascene or dual damascene wire in a fluorinated silicon glass dielectric layer, a top surface of said copper damascene or dual damascene wire coplanar with a top surface of said fluorinated silicon glass dielectric layer;

a first capping layer formed on said top surface of said copper damascene or dual damascene wire and said top surface of said fluorinated silicon glass dielectric layer; and

a second capping layer formed on said top surface of said first capping layer, said first capping layer thin enough to allow performance of one or more characterization procedures in relation to said ~~integrated circuit~~ structure and thick enough to prevent formation, on said top surface of said copper damascene or dual damascene wire, of copper containing particles by reaction of copper in said copper damascene or dual damascene wire with fluorine in said fluorinated silicon glass dielectric layer.

40. (Currently Amended) The structure of claim ~~38~~ 39, wherein said fluorinated silicon glass dielectric layer comprises about 1% to about 9% by weight of fluorine.

41. (Currently Amended) The structure of claim ~~38~~ 39, wherein said first capping layer and said second capping layer independently include a material selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

42. (Currently Amended) The structure of claim ~~38~~ 39, wherein said first capping layer and said second capping layer independently include one or more layer of materials selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

43. (Currently Amended) The structure of claim ~~38~~ 39, wherein said first capping layer has a thickness between about 100 Å and 300 Å.

44. (Currently Amended) The ~~method~~ structure of claim ~~38~~ 39, wherein said second capping layer has a thickness between about 150 Å and 700 Å.

45. (Currently Amended) The ~~method~~ structure of claim ~~38~~ 39, wherein said second capping layer is a copper diffusion barrier.

46. (Currently Amended) The ~~method~~ structure of claim ~~38~~ 39, wherein said first capping layer in combination with said second capping layer is a copper diffusion barrier.

47. (Currently Amended) The ~~method~~ structure of claim ~~38~~ 39, wherein said one or more characterization procedures are selected from the group consisting of optical or SEM inspection, optical or SEM image size measurement and electrical probing.

48. (Currently Amended) The ~~method~~ structure of claim ~~38~~ 39, wherein said first capping layer is thin enough to be transparent to visible light, to back-scattered electrons in a SEM or to both.

49. (Currently Amended) The ~~method~~ structure of claim ~~38~~ 39, wherein said first capping layer is thin enough to allow penetration of said first capping layer by a point of a conductive probe tip in order to make electrical contact to said copper damascene or dual damascene wire.

50. (Original) A method of manufacturing an interconnect, comprising:

(a) providing a substrate;

(b) forming a copper wire in a dielectric layer, said dielectric layer having a top surface;

(c) exposing a copper top surface of said copper wire, said copper top surface of said copper wire coplanar with said top surface of said dielectric layer or exposing said copper top surface of said copper wire in a bottom of a trench formed in said dielectric layer;

after step (c), (d) storing said substrate in a controlled environment; and

after step (d), (e) performing further processing steps on said substrate.

51. (Currently Amended) The method of claim ~~49~~ 50, wherein said dielectric layer comprises fluorinated silicon glass.

52. (Currently Amended) The method of claim ~~49~~ 50, wherein said controlled environment is selected from the group consisting of humidity controlled environment, temperature controlled environments, inert gas environments, non-oxygen containing environments and combinations thereof.

53. (Currently Amended) The method of claim ~~49~~ 50, wherein said controlled environment has a relative humidity of about 20% or less at a temperature of about 70°F or less.

54. (Currently Amended) The method of claim ~~49~~ 50, wherein said controlled environment comprises H_2, He, Ar, N_2, combinations H_2, He, Ar, N_2, or air with a relative humidity of about 20% or less.

55. (Original) A method of manufacturing an interconnect, comprising:

(a) providing a substrate;

(b) forming a copper wire in a dielectric layer, said dielectric layer having a top surface;

(c) exposing a copper top surface of said copper wire, said copper top surface of said copper wire coplanar with said top surface of said dielectric layer or exposing said copper top surface of said copper wire in a bottom of a trench formed in said dielectric layer to an ambient atmosphere for a period of time;

after step (c), (d) if said period of time exceeds a predetermined period of time, performing a rework clean or a rework chemical mechanical polish; and

after step (d), (e) performing further processing steps on said substrate.

56. (Currently Amended) The method of claim ~~54~~ 55, wherein said dielectric layer comprises fluorinated silicon glass.

57. (Currently Amended) The method of claim 54 55, wherein step (e) includes forming a capping layer over said dielectric layer.

58. (Currently Amended) The method of claim ~~54~~ 55, wherein said rework clean includes etching in an aqueous solution containing HF.

59. (Currently Amended) The method of claim ~~54~~ 55, wherein formation of said copper wire includes a first chemical mechanical polish of a copper layer formed over a non-copper liner layer followed by a second chemical mechanical polish of said liner layer; and

wherein said rework chemical mechanical polish is the same process as said second chemical mechanical polish for about the same or less time.

60. (Currently Amended) The method of claim ~~54~~ 55, further including:

after step (c), (f) determining an elapsed time from formation of said capping layer to a present time;

after step (f), (g) if said elapsed time exceeds a additional predetermined period of time, performing a cryogenic clean; and

after step (g), (h) forming an additional capping layer on a top surface of said capping layer.